ABSTRACT

A method and apparatus for overflow detection and clamping with parallel operand processing for fixed-point multipliers is disclosed. The invention predicts when a multiplication of a number of operands will exceed a pre-determined number of bits based upon the fixed-point format of the operands. The prediction is performed in parallel with the multiplication of the operands. The multiplication need not be completed in full, but only to the extent to determine whether overflow exists. If an overflow detection occurs, clamping is instituted. The parallel operation of the overflow detection and the multiplication provides a faster clamping circuit than would otherwise be available from a serial multiplication followed by a clamping analysis.